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Docket No.: 04303/100N133-US1
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Letters Patent of:
Joel D. Medlock

Patent No.: 6,895,036

Issued: May 17, 2005

For: APPARATUS AND METHOD FOR SUB-CHIP OFFSET CORRELATION IN SPREAD-SPECTRUM COMMUNICATION SYSTEMS

REQUEST FOR CERTIFICATE OF CORRECTION
PURSUANT TO 37 CFR 1.322

Attention: Certificate of Correction Branch
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Upon reviewing the above-identified patent, Patentee noted an error which should be corrected.

In the Specification:

Column 4, Line 3, Delete "fall" and insert -- full --.

Column 5, Line 33, Delete "205" and insert --205K --.

The error was not in the application as filed by applicant; accordingly no fee is required.

Enclosed please find copies of pages 5 & 6 of the Specification.

Transmitted herewith is a proposed Certificate of Correction effecting such amendment. Patentee respectfully solicits the granting of the requested Certificate of Correction.

Dated: July 26, 2005

Respectfully submitted,

By_____

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UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO.	:	6,895,036
APPLICATION NO.	:	09/772,580
ISSUE DATE	:	May 17, 2005
INVENTOR(S)	:	Joel D. Medlock

It is certified that an error appears or errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In the Specification:

Column 4, Line 3, Delete "fall" and insert -- full --.

Column 5, Line 33, Delete "205" and insert --205K --.

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205

that may compromise the accuracy of the search procedure include non-identical spreading codes, frequency offset, correlation window size less than the full period of the spreading code, etc.

In a conventional searcher, incoming data is correlated with a locally generated pseudorandom noise (PN) sequence. The incoming data is delayed by a fraction of a chip and the delayed data is correlated with the locally generated PN sequence. In a conventional searcher, the two correlation results are analyzed separately and the analysis result is used in detecting a code match.

According to the present invention, further reduction of the "miss" probability can be achieved if data streams that are offset by a fraction of a chip are added and correlated as opposed to correlating each sub-chip offset data stream individually.

Furthermore, the average time for achieving code acquisition may also be substantially reduced. The equation for the time average of the autocorrelation function is given as:

$$\text{Time average of autocorrelation} = [1-(1+\frac{1}{N})\times\frac{|\varepsilon|}{T_c}]^2$$

where N is the sequence length, ε is the sub-chip offset in fractions of a chip, and T_c is one chip period. As can be seen from the equation, reducing the sub-chip offset will reduce the time average of autocorrelation.

Although "miss" probability can be significantly reduced by using techniques of the present invention, precision may be compromised. Each result combines at least two sub-chip sequences and the phase uncertainty is twice the sub-chip offset. Thus, the technique of the present invention should be used for coarse searching.

Communication Device in Accordance with the Present Invention

Figure 1 is a block diagram of a spread spectrum communication device in accordance with one embodiment of the present invention. Electronic communication device 100a may be part of a wireless mobile handset. Electronic communication device 100a may also be a part of a wireless base station, an embedded wireless modem, a test platform, or other communication device. Electronic communication device 100a may also be any electronic device that performs a function of identifying a phase offset of a signal with a known data sequence, e.g., a pilot signal.

As illustrated in Figure 1, communication device 100a includes an antenna 101 coupled to a front-end processing block 103 to receive a wireless signal. Front-end processing block 103 includes components such as a radio frequency (RF) transceiver (not

shown) and an analog to digital (A/D) converter (not shown), coupled to each other in series. The components and functions of the front-end processing block 103 are known to those skilled in the art. Front-end processing block 103 is coupled to a base band processor 106a and a bus 116, to which a memory 104 and a processor (or controller) 110 are also coupled.

Base band processor 106a, which is operable to process the base band portion of the received signal, includes components such as modem processors 108a and 108b, a channel codec processor 114, and a searcher 120. Base band processor 106a also includes a code generator 113 coupled to the searcher 120. It is appreciated that modem processors 108a and 108b, codec processor 114, and code generator 113 have components that are known to those skilled in the art.

Searcher 120 is a device that performs the function of correlating incoming data with locally generated code sequences. When a correlation is found, the communication device 100a is synchronized with the incoming data. In particular, the searcher 120 of the present embodiment performs a sub-chip correlation. By performing sub-chip correlation, searcher 120 is able to improve overall performance of communication device 100a.

While communication device 100a provides a specific quantity of components that are arranged in a specific configuration, the present invention is well suited to a wide range of alternatives. For example, a single modem processor is used in one embodiment, while another embodiment utilizes greater than two modem processors, coupled to searcher 120. Furthermore, communication device 100a is adaptable to a wireless system utilizing code division multiple access (CDMA) protocol in one embodiment. However, communication device 100a is well suited to other spread spectrum communication protocols.

Apparatus for Performing Sub-chip Offset Correlation

Figure 2A is a block diagram illustrating an apparatus 200a for performing sub-chip correlation in accordance with an embodiment of the present invention. The apparatus 200a may be implemented as part of the searcher 120 of communication device 100a. As illustrated, an input data stream (from front end processing 130) is received on bus 203 and is applied to a plurality of sub-chip delay circuits 205a-205k. The sub-chip delay circuits (except circuit 205k) each generate a data stream that is offset by a fraction of a chip with respect to the input data. For example, the sub-chip delay circuit 205a generates a data stream that is offset by 1/k of a chip with respect to the input data stream, and the sub-chip delay circuit 205b generates another data stream that is offset by 2/k of a chip with respect to the input data stream. The sub-chip delay circuit 205k generates data that is offset by one chip. It should be appreciated that the sub-chip delay circuits may be implemented as a

Application No. (if known): 09/772,580 Attorney Docket No.: 04303/100N133-US1

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on July 26, 2005
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Lillian Garcia
Signature

Lillian Garcia
Typed or printed name of person signing Certificate

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